Amendments to the Claims

This listing of claims will replace all prior versions, and listings of claims in the application.

Claims 1-7. Cancelled

8. (Original) Simulation system for simulation of an electronic circuit, the circuit being representable by a network of logical elements, the circuit comprising first and second asynchronous clock domains, wherein jitter elements are additionally insertable at predetermined portions of circuit boundaries between the first and second clock domains, the jitter elements being representable as logical elements, the values of which are randomly set.

9. (Original) The system of claim 8, wherein the simulation is carried out on cycle level of a description of the electronic circuit.

10. (Original) The system of claim 8, wherein the jitter elements comprise delay elements for introducing predetermined timing delays which is randomly exercised.

11. (Original) The system of claim 8, wherein the jitter elements comprise x generator elements for introducing predetermined signal values which are randomly generated.

12. (Original) The system of claim 8, wherein the jitter elements are interactively inserted by a user.

13. (Original) The system of claim 8, wherein the jitter elements are automatically inserted using predetermined modules.

Claims 14. - 15. Cancelled